## Institute of Computer Science/Information Technology (ICS&IT) Faculty of Management Sciences & Computer Sciences (FMCS) The University of Agricultural Peshawar

Program:	BS(CS)-II
Course Name:	Digital Logic Design
Course Code :	CC-312
Course Hours :	03
Total Weeks :	16
Total Hours :	48

### Course Objectives:

This course covers the topics, which provides the students the basic concept of switching theory and digital design. After studying this course the students will be able to understand the working principle and design of digital systems. It includes the following topics which prepare the students for the design of circuits used in micro computer: number system, computer codes, logic gates, Boolean algebra, combinational logic circuits, flip flops, registers, counters, memories, and microprocessor etc.

This course will help and prepare the students to take advance courses in computer architecture in future.

# NUMBER SYSTEMS, OPERATIONS, AND CODES

Week-1

- Decimal Numbers
- Binary Numbers
- Binary to Decimal Conversion
- Binary Arithmetic
- 1's and 2's Compliments of Binary Numbers

### Week-2

- Signed Numbers
- Arithmetic Operations with Signed Numbers
- Hexadecimal Numbers
- Octal Numbers
- Binary Coded Decimal (BCD)
- Digital Codes and Parity

## Week-3

## LOGIC GETES

- The Inverter (NOT Gate)
- The AND Gate
- The OR Gate
- The NAND Gate
- The NOR Gate
- The X-OR and X-NOR Gate

# BOOLEAN ALGEBRA AND LOGIC SIMPLIFICATION

# Week-4

<ul> <li>Laws and Rules of Boolean Algebra De-Morgan's Theorems</li> <li>Week-5</li> <li>Boolean Analysis of Logic Circuits</li> <li>Simplification using Boolean Algebra</li> <li>Week-6</li> <li>Standard Forms of Boolean Expressions Boolean Expressions and Truth Tables</li> <li>Week-7</li> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Functional Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9</li> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> <li>Week-10</li> <li>Decoders</li> <li>Encoders</li> </ul>	
<ul> <li>De-Morgan's Theorems</li> <li>Week-5</li> <li>Boolean Analysis of Logic Circuits</li> <li>Simplification using Boolean Algebra</li> <li>Week-6</li> <li>Standard Forms of Boolean Expressions</li> <li>Boolean Expressions and Truth Tables</li> <li>Week-7</li> <li>The Karnaugh Map</li> <li>Karnaugh Map POS Minimizations</li> <li>Week-8</li> <li>Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>Parallel Binary Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> <li>Week-10</li> <li>Decoders</li> <li>Encoders</li> <li>Encoders</li> <li>Karnaugh Map POS Minimizations</li> </ul>	
Week-5       Boolean Analysis of Logic Circuits         Simplification using Boolean Algebra         Week-6         Boolean Expressions and Truth Tables         Week-7         The Karnaugh Map         Karnaugh Map SOP Minimizations         Karnaugh Map POS Minimizations         Karnaugh Map POS Minimizations         Week-8         COMBINATIONAL LOGIC         Basic Combinational Logic Circuits         Implementing Combinational Logic         The Universal Property of NAND and NOR Gates         Combinational Logic Using NAND and NOR Gates         Combinational Logic Using NAND and NOR Gates         PunCTIONS OF COMBINATIONAL LOGIC         Week-9         Basic Adders         Parallel Binary Adders         Parallel Binary Adders         Comparator         Week-10         Decoders         Encoders         Encoders	
Week-5       Boolean Analysis of Logic Circuits         Simplification using Boolean Algebra         Week-6         Standard Forms of Boolean Expressions         Boolean Expressions and Truth Tables         Week-7         The Karnaugh Map         Karnaugh Map SOP Minimizations         Karnaugh Map POS Minimizations         Karnaugh Map POS Minimizations         Basic Combinational Logic Circuits         Implementing Combinational Logic         The Universal Property of NAND and NOR Gates         Combinational Logic Using NAND and NOR Gates         FUNCTIONS OF COMBINATIONAL LOGIC         Week-9         Basic Adders         Parallel Binary Adders         Parallel Binary Adders         Comparator         Week-10         Decoders         Encoders         Encoders	
<ul> <li>Boolean Analysis of Logic Circuits</li> <li>Simplification using Boolean Algebra</li> <li>Week-6 <ul> <li>Standard Forms of Boolean Expressions</li> <li>Boolean Expressions and Truth Tables</li> </ul> </li> <li>Week-7 <ul> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Karnaugh Map POS Minimizations</li> </ul> </li> <li>Week-8 <ul> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> </ul> </li> <li>Week-9 <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10 <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul>	
<ul> <li>Bootean Analysis of Eogle Circuits</li> <li>Simplification using Boolean Algebra</li> <li>Week-6         <ul> <li>Standard Forms of Boolean Expressions</li> <li>Boolean Expressions and Truth Tables</li> </ul> </li> <li>Week-7         <ul> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Karnaugh Map POS Minimizations</li> </ul> </li> <li>Week-8         <ul> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> </ul> </li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> <li>Week-10             <ul> <li>Decoders</li> <li>Encoders</li> <li>Week-11</li> </ul> </li> </ul></li></ul>	
<ul> <li>Simplification using Boolean Algebra</li> <li>Week-6</li> <li>Standard Forms of Boolean Expressions</li> <li>Boolean Expressions and Truth Tables</li> <li>Week-7</li> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Week-8</li> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9</li> <li>Basic Adders</li> <li>Comparator</li> <li>Week-10</li> <li>Decoders</li> <li>Encoders</li> <li>Week-11</li> </ul>	
<ul> <li>Week-6 <ul> <li>Standard Forms of Boolean Expressions</li> <li>Boolean Expressions and Truth Tables</li> </ul> </li> <li>Week-7 <ul> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Karnaugh Map POS Minimizations</li> </ul> </li> <li>Week-8 <ul> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> </ul> </li> <li>Week-9 <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10 <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul>	
<ul> <li>Week-6 <ul> <li>Standard Forms of Boolean Expressions</li> <li>Boolean Expressions and Truth Tables</li> </ul> </li> <li>Week-7 <ul> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> </ul> </li> <li>Week-8 <ul> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> </ul> </li> <li>Week-9 <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10 <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul>	
<ul> <li>Standard Forms of Boolean Expressions Boolean Expressions and Truth Tables</li> <li>Week-7         <ul> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> </ul> </li> <li>Week-8         <ul> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> </ul> </li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Comparator</li> <li>Week-10             <ul> <li>Decoders</li> <li>Encoders</li> <li>Encoders</li> <li>Encoders</li> <li>Encoders</li> </ul> </li> </ul></li></ul>	
<ul> <li>Boolean Expressions and Truth Tables</li> <li>Week-7         <ul> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> </ul> </li> <li>Week-8         <ul> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> </ul> </li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> <li>Week-10             <ul> <li>Decoders</li> <li>Encoders</li> <li>Encoders</li> <li>Encoders</li> <li>Encoders</li> </ul> </li> </ul></li></ul>	
<ul> <li>Week-7 <ul> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> </ul> </li> <li>Week-8 <ul> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> </ul> </li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9 <ul> <li>Basic Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10 <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul>	
<ul> <li>Week-7 <ul> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> </ul> </li> <li>Week-8 <ul> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> </ul> </li> <li>Week-9 <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10 <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul>	
<ul> <li>The Karnaugh Map</li> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Week-8</li> <li>COMBINATIONAL LOGIC</li> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9</li> <li>Basic Adders</li> <li>Comparator</li> <li>Week-10</li> <li>Decoders</li> <li>Encoders</li> </ul>	
<ul> <li>Karnaugh Map SOP Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Week-8 COMBINATIONAL LOGIC         <ul> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> </ul> </li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Comparator</li> <li>Week-10</li> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul>	
<ul> <li>Kanadgi Map Sof Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Karnaugh Map POS Minimizations</li> <li>Week-8 COMBINATIONAL LOGIC         <ul> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> </ul> </li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> <li>Week-10             <ul> <li>Decoders</li> <li>Encoders</li> <li>Week-11</li> </ul> </li> </ul></li></ul>	
<ul> <li>Kanadgh Map POS Minimizations</li> <li>Week-8 COMBINATIONAL LOGIC         <ul> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> </ul> </li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> <li>Week-10             <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul></li></ul>	
<ul> <li>Week-8 COMBINATIONAL LOGIC <ul> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> </ul> </li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9 <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10 <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul>	
<ul> <li>Week-8 COMBINATIONAL LOGIC <ul> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> </ul> </li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9 <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10 <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul>	
<ul> <li>Basic Combinational Logic Circuits</li> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10         <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> <li>Week-11</li> </ul>	
<ul> <li>Implementing Combinational Logic</li> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10         <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> <li>Week-11</li> </ul>	
<ul> <li>The Universal Property of NAND and NOR Gates</li> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10         <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> <li>Week-11</li> </ul>	
<ul> <li>Combinational Logic Using NAND and NOR Gates</li> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10         <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> <li>Week-11</li> </ul>	
<ul> <li>FUNCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9         <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10         <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> <li>Week-11</li> </ul>	
FUNCTIONS OF COMBINATIONAL LOGIC         Week-9         -       Basic Adders         -       Parallel Binary Adders         -       Comparator         Week-10       -         -       Decoders         -       Encoders         -       Encoders	
<ul> <li>FORCTIONS OF COMBINATIONAL LOGIC</li> <li>Week-9 <ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> </ul> </li> <li>Week-10 <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> <li>Week-11</li> </ul>	
<ul> <li>Week-9</li> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> <li>Week-10</li> <li>Decoders</li> <li>Encoders</li> </ul>	
<ul> <li>Basic Adders</li> <li>Parallel Binary Adders</li> <li>Comparator</li> <li>Week-10 <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> </ul>	
<ul> <li>Parallel Binary Adders</li> <li>Comparator</li> <li>Week-10         <ul> <li>Decoders</li> <li>Encoders</li> </ul> </li> <li>Week-11</li> </ul>	
- Comparator Week-10 - Decoders - Encoders	
Week-10 - Decoders - Encoders Week-11	
- Decoders - Encoders Week-11	
- Encoders Week-11	
Week-11	
Week-11	
Week-11	
- Multiplexer	
- Demultiplexer	
Week-12 FLIP-FLOPS AND RELATED DEVICES	
- Latches	
Edge-Triggered Elin-Elons	
- Euge-Higgered Hip-Hops	
- Master-Slave Flip-Flops	
Week-13 COUNTERS	
- Asynchronous Counter Operation	
- Synchronous Counter Operation	
• I	
SHIFT REGISTERS	
- Asynchronous Counter Operation	

### Week -14

- Basic Shift Register Functions
- Serial In/Serial Out Shift Register
- Serial In/parallel Out Shift Register

### Week-15

- Parallel In/Serial Out Shift Register
- Parallel In/Parallel Out Shift Register

# Week-16 MICROPROCESSOR AND MEMORY/STORAGE DEVICES

- Random Access Semiconductor Memories
- Magnetic and optical Storage devices
- Introduction to Microprocessor and Microcomputer

## **RECOMMENDED BOOK:**

DIGITAL FUNDAMENTALS 7<sup>th</sup> Edition, <u>Thomas L. Floyd</u> Prentice-Hall International, Inc.

### **REFERENCE BOOKS**:

- 1. DIGITAL COMPUTER ELECTRONICS by Malvino
- 2. COMPUTER LOGIC DESIGN by M. Morris Mano